Seunggeun Kim

sgkim@utexas.edu seunggeunkimkr.github.io Seunggeun Kim

Summary

I am a 3rd-year Ph.D. student majoring in Electrical and Computer Engineering at the University of Texas at Austin. My research interests are in the area of Machine Learning for Electrical Design Automation (ML4EDA) and generative modeling especially using diffusion models.

Education

PhD **University of Texas at Austin**, Electrical and Computer Engineering — Aug 2023 – Present
- Advisor: David Z. Pan

BS **Seoul National University**, Electrical and Computer Engineering — Mar 2017 – Feb 2023
- GPA: 3.9/4.0 (summa Cum Laude)
- 2 years absence to fulfill military duty

Publications

Fine-Tuning Masked Diffusion for Provable Self-Correction, **Under Review**

Seunggeun Kim*, Jaeyeon Kim*, Taekyun Lee*, David Z. Pan, Hyeji Kim, Sham Kakade, Sitan Chen

PPAAS: PVT and Pareto Aware Analog Sizing via Goal-conditioned Reinforcement Learning, **ICCAD 2025**

Seunggeun Kim, Ziyi Wang, Sungyoung Lee, Youngmin Oh, Hanqing Zhu, Doyun Kim, David Z. Pan

Addressing Continuity and Expressivity Limitations in Differentiable Physical Optimization: A Case Study in Gate Sizing, **ISEDA 2025**

Yufan Du, Zizheng Guo, Yang Hsu, Zhili Xiong, **Seunggeun Kim**, David Z Pan, Runsheng Wang, Yibo Lin

DICE: Device-level Integrated Circuits Encoder with Graph Contrastive Pretraining, **Under Review**

Sungyoung Lee, Ziyi Wang, **Seunggeun Kim**, Taekyun Lee, Yao Lai, David Z. Pan

M3: Mamba-assisted Multi-Circuit Optimization via MBRL with Effective Scheduling, **ICCAD 2025**

Youngmin Oh, Jinje Park, **Seunggeun Kim**, Taejin Paik, David Pan, Bosun Hwang

LLM-enhanced Bayesian optimization for efficient analog layout constraint generation, **arXiv preprint**

Guojin Chen, Keren Zhu, **Seunggeun Kim**, Hanqing Zhu, Yao Lai, Bei Yu, David Z Pan

Experience

Samsung AI Center, Research Intern — Suwon, Korea, May 2024 – Jul 2024
- Mentor: Doyun Kim
- Reinforcement Learning for PVT-aware analog sizing

Seoul National University, Research Intern — Seoul, Korea, Jan 2021 – Jul 2023
- Advisor: Jaeha Kim
- Project lead of DSP tape-out with Samsung 14nm FinFET technology

Honors and Awards

DAC Young Fellowship — 2024
UT Austin Engineering Fellowship — 2023

Technologies

Programming Languages: Python, Verilog, C, C++, Java

Technologies: Pytorch, Tensorflow, Linux, GIT

Circuit Tools: Virtuoso, Spectre, Design Compiler, Vivado, XMODEL, NGSpice